Notice of Allowability	Application No. 10/675,027	Applicant(s) KIM ET AL.	
	Examiner VINEETA S. PANWALKAR	Art Unit 2611	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address–

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *telephone interview regarding examiner's amendment dates 8/20/09*.

2. ☒ The allowed claim(s) is/are *1,3,5-8,10-24,30,34-38, now renumbered 1-27*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Kirk DeNiro (Reg. No. 35854) on 8/20/09.

The application has been amended as follows:

2. **In the claims:**

a. Replace claim 1 with:

1) (Currently Amended) A circuit, comprising:

a clock circuit capable of generating a clock signal having a phase, the clock circuit including a phase adjuster capable of making an adjustment to the phase of the clock signal during each of a plurality of adjustment cycles in response to an adjustable phase step-size;

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate by outputting sampled data bits as received data signal; and

wherein the circuit further includes phase detection and logic circuitry capable of stalling adjustment of the phase of the clock signal during one or more current adjustment cycles in response to data phase

information derived from a plurality of data bits during one or more previous adjustment cycles,

wherein the circuit further includes a phase adjust step-size logic capable of outputting the adjustable phase step-size having an adjustable magnitude dependent on the variable data bit-rate. --

2b. Cancel claim 2.

2c. Replace claim 3 with:

--3) (Currently Amended) The circuit of claim 1, wherein the phase adjust step-size logic is capable of outputting the adjustable phase step-size having a direction dependent on the variable data bit-rate. --

2d. Replace claim 10 with:

--10) (Currently Amended) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to an adjustable phase step-size; and

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate,

wherein the circuit includes an indicator capable of adjusting the adjustable phase step-size in response to the variable data bit-rate,

wherein the circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step-size and the second step-size are summed to obtain the adjustable phase step-size --

e. Replace claim 12 with:

--12) (Currently Amended) The circuit of claim 1, wherein the circuit includes an averaging circuit capable of averaging a plurality of up signals to obtain an average up value and a plurality of down signals to obtain an average down value, and outputting the adjustable phase step-size in response to a comparison of the average up value and the average down value. --

2f. Replace claim 14 with:

--14) (Currently Amended) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to a phase adjust signal;

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate; and,

wherein the circuit comprises,

a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to a sampled data signal;

a second stage, coupled to the first stage, capable

of outputting a second stage output signal in response to the first stage output signal;

a third stage capable of outputting the phase adjust signal in response to the second stage output signal; and;

stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second stage output signals.

2g. Replace claim 18 with:

--18) (currently amended) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to a phase adjust signal having an adjustable step-size; and,

a sampler capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate;
wherein the circuit includes,
a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to a sampled data signal;
a second stage, coupled to the first stage, capable
of outputting a second stage output signal in response to the first stage output signal;
a third stage capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal;
stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals;
an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit-rate; and,
a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having the adjustable step-size in response to the first and second step-sizes. --

h. Introduce new claim 34 as follows:

34. (New) The method of claim 30, wherein the signal is received in response to a clock signal and wherein the update rate is a divisor of a frequency of a clock signal. --

i. Introduce new claim 35 as follows:

35) (New) The method of claim 30, further comprising determining phase information associated with the plurality of digital data signals including:
deserializing the plurality of digital data signals to output a group of data bits in parallel;

comparing phases of the of the group of digital data bits with a phase of a clock signal to generate the plurality of up signals and the plurality of down signals; and determining the phase information based on the plurality of up signals and the plurality of down signals. --

2j. Introduce new claim 36 as follows:

--36) (New) The method of claim 30, wherein the signal is a data signal having the variable data bit-rate and the signal is received in response to the clock signal and further comprising:
updating a phase of the clock signal based on the adjustable step size. --

2k. Introduce new claim 37 as follows:

--37) (New) The circuit of claim 1, wherein the circuit includes multiple pipelined stages that are controlled by a timing signal having a frequency that is a divisor of a frequency of the clock signal. --

2l. Introduce new claim 38 as follows:

--38) (New) The circuit of claim 1, wherein the circuit further comprises a de-serializer coupled between an output of the sampler and the clock circuit, and wherein the circuit compares phases of a plurality of data bits output from the de-serializer with the phase of the clock signal to generate a plurality of up signals and a plurality of down signals, the circuit derives the data phase information based on the plurality of up signals and the plurality of down signals. --

3. **In the specifcation:**

3a. In line 13 on Page 3 of the specification, replace "the Clock circuit" with "the circuit"

3b. In line 20 on Page 3 of the specification, replace "the Clock circuit" with --the circuit --.

3c. In line 22 on Page 3 of the specification, replace "the Clock circuit" with --the circuit --.

3d. Replace the Abstract with:

-- A circuit, such as a CDR circuit, includes a sampler to receive a data signal having a variable data bit-rate responsive to a clock signal in an embodiment of the present invention. A clock circuit is coupled to the sampler and generates the clock signal responsive to a selectable update rate and a selectable phase adjust step-size. In a second embodiment of the present invention, the circuit includes a Stall logic that is coupled to first, second and third stages and is capable to hold the phase adjust signal responsive to the first and second stage output signals. In a third embodiment of the present invention, an indicator detects the variable data bit-rate and a counter provides the selectable phase adjust step-size for the adjust signal. In a fourth embodiment of the present invention, the circuit includes the Stall logic, the indicator and the counter. In a fifth embodiment of the present invention, the circuit includes an Averaging circuit to output a phase adjust signal responsive to the averaging of a first and second adjust signals for a predetermined period of time. --

Allowable Subject Matter

4. Claims 1, 4, 5-8, 10-24, 30 and 35-38 as per examiner's amendment above are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

4a. Regarding claim 1, prior art of record fails to show the circuit, wherein the clock circuit includes a phase adjust step-size logic capable of outputting an adjustable magnitude of the phase step-size in response to the variable data bit-rate, in combination with every other limitation of the claim.

4b. Claim 3, 5-8, 12, 13, 37 and 38 are allowed as being dependent on claim 1.

4c. Regarding claim 10, prior art of record fails to show the circuit wherein the clock circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step size and the second step size are summed to obtain the adjustable phase step-size, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs. 1 and 7.

4d. Claim 11 is allowed as being dependent on claim 10.

4e. Regarding claim 14, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable a second stage output signal in response to the first of outputting stage output signal, a third stage, coupled to the second stage, capable outputting the phase adjust signal in response to the second stage output signal; and stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second

stage output signals, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

4f. Claims 15-17 are allowed as being dependent on claim 14.

4g. Regarding claim 18, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal; a third stage, coupled to the second stage, capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal; stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals; an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit- rate; and, a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having an adjustable step-size responsive to the first and second step-sizes, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1, 5 and 7.

4h. Claims 19-24 are allowed as being dependent on claim 18.

4i. Regarding claim 30, prior art of record fails to show a method for tracking signals wherein selecting an adjustable step-size includes determining a first step-size based on a variable data bit-rate of the signal; determining a second step-size

and summing the first and second step sizes to obtain adjustable the step-size, in combination with each and every other limitation of the claim.

4j. Claims 34, 35 and 36 are allowed as being dependent on claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINEETA S. PANWALKAR whose telephone number is (571)272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/V. S. P./
Examiner, Art Unit 2611

/Mohammad H Ghayour/
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